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# APPLICATION FOR LETTERS PATENT

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# Non-Volatile Resistance Variable Devices And Method of Forming Same, Analog Memory Devices And Method of Forming Same, Programmable Memory Cell And Method Of Forming Same, And Method of Structurally Changing a Non-Volatile Device

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INVENTOR

Terry L. Gilton

ATTORNEY'S DOCKET NO. MI22-1480

# Non-Volatile Resistance Variable Devices And Method of Forming Same, Analog Memory Devices And Method of Forming Same, Programmable Memory Cell And Method Of Forming Same, And Method of Structurally Changing a Non-Volatile Device

## TECHNICAL FIELD

This invention relates to non-volatile resistance variable devices, to analog memory devices, to programmable memory cells, and to methods of forming such devices, to programming such devices and structurally changing such devices.

## BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as

a programmable metallization cell. Such a cell includes opposing electrodes having an insulating dielectric material received therebetween. Received within the dielectric material is a fast ion conductor material. The resistance of such material can be changed between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a chemical and structural change at a certain applied voltage. Specifically, at some suitable threshold voltage, plating of metal from metal ions within the material begins to occur on the cathode and grows or progresses through the fast ion conductor toward the other anode electrode. With such voltage continued to be applied, the process continues until a single conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the

anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The highly conductive filament which forms between the illustrated electrodes in the fast ion conductor material tends to form at a surface thereof, as opposed to centrally within the mass of material. It has been discovered that defects on such surface somehow create an electrochemical path of least resistance along which the conductive filament during programming will form. Accordingly, the forming filament may serpentine along a path of least resistance at the peripheral edge surface of the material between the two electrodes, thereby resulting in variability in the amount of time it takes to program two devices of otherwise common dimensions. It would be desirable to develop structures and methods which overcome this write time variability.

While principally motivated utilizing the above-described circuitry and addressing the stated specific objective, the invention is in no way so limited. Rather, the invention is more broadly directed to any non-volatile resistance variable devices, including methods of fabricating, programming and structurally changing the same, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the doctrine of equivalents.

## SUMMARY

The invention comprises non-volatile resistance variable devices, analog memory devices, programmable memory cells, and methods of forming such devices, programming such devices and structurally changing such devices. In one implementation, a non-volatile resistance variable device includes a body formed of a voltage or current controlled resistance setable material, and at least two spaced electrodes on the body. The body includes a surface extending from one of the electrodes to the other of the electrodes. The surface has at least one surface striation extending from proximate the one electrode to proximate the other electrode at least when the body of said material is in a highest of selected resistance setable states.

In one implementation, a method includes structurally changing a non-volatile device having a body formed of a voltage or current controlled resistance setable material and at least two spaced electrodes on the body. The body has a surface extending from one of the electrodes to the other of the electrodes, and the surface is formed to comprise at least one surface striation extending from proximate the one electrode to proximate the other electrode. The method includes applying a first voltage between the one and the other electrodes to establish a negative and a positive electrode effective to form a conductive path formed of at least some material derived from the voltage or current controlled resistance setable material and on the surface along at least a portion of the at least one striation.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1, and taken relative to line 2-2 in Fig. 3.

Fig. 3 is a diagrammatic top view of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 5 is a diagrammatic top view of a portion of Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a diagrammatic top view of a portion of Fig. 7.

Fig. 9 is a diagrammatic top view like Fig. 8, but showing an alternate embodiment from that of Fig. 8.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metallization cells and programmable optical elements of the patents referred to above, further by way of example only including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. Further by way of example only, the invention also contemplates forming non-volatile resistance variable devices into an analog memory device capable of being set and reset to a resistance value over a continuous range of resistance values which is measure of a voltage applied to it over a corresponding range of voltage values. By way of example only, such are disclosed in U.S. Patent No. 5,360,981, which resulted from a serial number application 194,628, filed on May 4, 1990, listing Owen et al. as inventors. This '981 patent is fully herein incorporated by reference. In the context of this document, the term "semiconductor substrate" or

"semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural. Further, it will be appreciated by the artisan that "resistance setable semiconductive material" and "resistance variable device" includes materials and devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the material's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A conductive first electrode material 16 is formed over dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. and/or Owen et al. patents referred to above, in conjunction with the preferred type of device being fabricated. A dielectric layer 18 is formed over first electrode layer 16. Silicon nitride is a preferred example.

Referring to Figs. 2 and 3, a masking layer 20, for example photoresist, is received over layer 18. An opening 22 is formed into masking layer 20 and dielectric layer 18 to first electrode layer 16. Opening 22 includes masking layer sidewalls 24 and dielectric layer sidewalls 26. Forming such opening is conducted in a manner which produces at least one surface striation 28 in at least a portion of opening sidewalls 26. Typically and preferably, a plurality of such surface striations 28 are formed, and preferably extend from proximate first electrode layer 14 along the substantial entirety of opening 22 within dielectric layer 18 to the outer surface thereof. Accordingly, in the most preferred embodiment, sidewall striations 28 extend in a substantially straight line, and preferably of least possible distance, from electrode layer 16 to the outermost surface of layer 18.

Most preferably, the forming of opening 22 within dielectric layer 18 is conducted by etching, and with sidewall striations 28 being formed during the initial dielectric layer 18 etching to form opening 22 therein. Alternately by way of example only, the manner of forming can comprise forming the at least one sidewall striation after dielectric layer 18 etching to initially form the opening and expose the electrode layer without significant striation forming therein. The illustrated and preferred manner comprises forming the at least one surface striation in sidewalls 24 of masking layer 20 which overlies dielectric layer 18, and thereafter etching into dielectric layer 18 to form opening 22

therein using masking layer 20 as an etching mask and thereby patterning the striations therefrom into opening 22 within layer 18.

Various techniques are known to the artisan for creating striations in a contact opening. By way of example only, such are disclosed in U.S. Patent No. 5,238,862 to Blalock et al., filed on March 18, 1992, and U.S. Patent Application Serial No. 09/492,738, filed January 27, 2000, entitled "Plasma Etching Methods", and listing Becker, Howard and Donahoe as inventors. These documents are herein fully incorporated by reference. The invention, of course, contemplates these and other striation-forming techniques, whether existing or yet-to-be developed.

Referring to Figs. 4 and 5, masking layer 20 has been removed and a voltage or current controlled resistance setable material is formed within opening 22 in layer 18 in electrical connection with first electrode layer 16. Example preferred materials include voltage or current controlled resistance setable semiconductive material, for example that disclosed in the Owen et al. patent referred to herein. Further, exemplary preferred material includes fast ion conductor material, such as metal ion-containing dielectric material or metal ion-containing semiconductive material, as disclosed in the Kozicki et al. patents referred to herein. Alternate materials are contemplated, of course, whether existing or yet-to-be developed. In the context of this document, voltage or current controlled resistance setable material includes any material whose resistance can be non-volatilely varied in

at least some manner by application of different voltages or currents therethrough.

Preferably as shown, such material 30 is formed to have a surface 32 at least a portion of which extends along the dielectric layer striations 28 to form at least one surface striation 34 (Fig. 5) in the surface portion of material 30. In the preferred and illustrated embodiment, the at least one surface portion striation 32 is received on dielectric layer 18 and therefore contacts the same. In the preferred embodiment, material 30 is shown as having been planarized relative to dielectric layer 18.

Referring to Fig. 6, a second electrode layer 40 is formed in electrical connection with voltage or current controlled resistance setable material 30 within opening 22 of dielectric 18. Accordingly, striations 34 of material 30 in the most preferred embodiment extend from proximate first electrode 16 to proximate second electrode 40, and most preferably in a substantially straight line of least possible distance therebetween. Fig. 6 depicts, in structure and method, an exemplary body 30 of voltage or current controlled resistance setable material having at least two spaced electrodes 16 and 40 received thereon. The body comprises a surface extending from one of the electrodes to the other of the electrodes, with the surface being formed to comprise at least one surface striation extending from proximate the one electrode to proximate the other electrode, at least when the body of the material is in a highest of selected resistance states. Fig. 6 illustrates

but one exemplary non-volatile resistance variable device, and a method of fabricating. Alternate methods and structures beyond that shown are, of course, contemplated. By way of example only, the various components could be laterally oriented relative to one another as opposed to successively deposited layers atop one another. Other orientations are, of course, contemplated.

The invention also contemplates methods of structurally changing a non-volatile device. The method comprises applying a first voltage between two electrodes to establish a negative and a positive electrode effective to form a conductive path formed of at least some material derived from voltage or current controlled resistance setable material received between the electrodes, and on the surface of such material along at least a portion of at least one striation formed therein. Such conductive path may extend partially between the electrodes, or alternately, entirely between the electrodes, effectively electrically shorting the electrodes together. The invention also comprises, after applying such first voltage, applying a second voltage opposite in polarity to the first voltage to reverse formation of the conductive path, either partially or entirely. The invention also comprises, after applying such first voltage, applying sufficiently high current to break the dendrite/filament. Exemplary techniques for accomplishing such are disclosed in the Kozicki et al. and Owen et al. patents.

The invention also contemplates fabrication and processing relative to analog memory devices capable of being set and reset to a resistance

value over a continuous range of resistance values, which is a measure of a voltage or current applied to it over a corresponding range of voltage or current values. An example is described in the Owen et al. patent.

Figs. 7, 8 and 9 illustrate exemplary embodiments involving programming or otherwise formation of a conductive path between the electrodes. For example, Figs. 7 and 8 illustrate a conductive path/dendrite 50 being formed in the sidewall portion of material 20 along an apex form of a striation 34. Fig. 9 illustrates an alternate embodiment wherein a conductive path/dendrite 50a forms at and along a valley portion of a striation 34. The invention also contemplates formation of a conductive path/dendrite anywhere along the surface between path 50 of Fig. 8 and path 50a of Fig. 9.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.